AMENDMENT TO THE CLAIMS

Please **AMEND** claims 6-10.

No new matter has been added. This listing of claims will replace all prior versions, and listings, of claims in the application.

In the Claims

1. (Previously Presented) A hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions, said device comprising:

a plurality of task units for processing data, making decisions and/or processing data and making decisions;

a task interconnection logic means interconnecting the task units for communicating actions from a source task unit to a destination task unit; and

each of said task units including a processor for executing the steps of the associated task in response to a received request action and a status manager for handling actions from source task units and building actions to be sent to destination task units.

2. (Previously Presented) The hardware device according to claim 1, wherein said actions communicated from a source task unit to a destination task unit are START used to activate the processor of said destination task unit, KILL used to cancel the task associated with said destination task unit and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said

task.

3. (Previously Presented) The hardware device according to claim 2, wherein said status manager activates said processor for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START.

4. (Previously Presented) The hardware device according to claim 3, wherein said status manager is a state machine.

5. (Previously Presented) The hardware device according to claim 3, wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow, each one of said control/data registers comprising a control field composed of a completion bitset to 1 when the associated task is completed, a validation bit set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision.

6. (Currently amended) The hardware device ~~according to claim 5,~~ for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions, said device comprising:

a plurality of task units for processing data, making decisions and/or processing data and making decisions; and

a task interconnection logic means interconnecting the task units for

communicating actions from a source task unit to a destination task unit; and

each of said task units including a processor for executing the steps of the associated task in response to a received request action and a status manager for handling actions from source task units and building actions to be sent to destination task units,

wherein said actions communicated from a source task unit to a destination task unit are START used to activate the processor of said destination task unit, KILL used to cancel the task associated with said destination task unit and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said task,

wherein said status manager activates said processor for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START, and

wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow, each one of said control/data registers comprising a control field composed of a completion bitset to 1 when the associated task is completed, a validation bit set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision, and

wherein each of said control/data registers includes a data field which is loaded if necessary by said status manager activated by an action received from a source task

unit, said processor using these data for executing the task associated with said task unit and replacing them if necessary.

7. (Currently amended) The hardware device according to claim [[6]] 5, wherein said completion bit is sent by said processor to said status manager after completion of the task execution.

8. (Currently amended) The hardware device according to claim 5[[, 6 or 7]], wherein said control/data register corresponding to a specific instance is cleared by said status manager when this one receives an action KILL for the task associated with said task unit and for said specific instance.

9. (Currently amended) The hardware device according to ~~any one of~~ claim[[s]] 5 [[to 7]], wherein each one of said task units further comprises two configuration registers CONFIG.L and CONFIG.R which are respectively selected by the binary value of said bit L/R of the control/data register of the instance being considered, the contents of said configuration registers being loaded at the beginning of the algorithm processing for defining the task to be activated, the action to be performed and the instance to be considered.

10. (Currently amended) The hardware device according to ~~any one of claims 1 to 7~~ claim 5, wherein said task interconnection logic means is composed of three-state drivers each one of said drivers being associated with one of said tasks as input task and a number of buses equal to the number of said tasks as output tasks, one of said buses being selected by the driver corresponding to an input task after decoding an action word by said driver.

11. (Previously Presented) The hardware device of claim 1, wherein each task unit of the plurality of task units is configured to perform only one task of the plurality of tasks associated with the algorithm.

12. (Previously Presented) A hardware device for concurrently processing a plurality of tasks associated with an algorithm, comprising:

at least two task units each configured to process the steps of a respective single task of a multiple task algorithm;

at least two processors configured to execute the respective single task in each of the respective at least two task units;

an interconnection logic means for routing actions from a source task unit to a destination task unit of the at least two task units, respectively; and

at least two status managers each being associated with each of the at least two task units, respectively, the at least two status managers configured to receive from the interconnection logic means the actions and directing execution of the respective single task.

13. (Previously Presented) The hardware device of claim 12, wherein each of the task units repetitively perform only its respective single task.

14. (Previously Presented) The hardware device of claim 12, wherein the status manager handles incoming commands for other task units of the at least two task units and builds commands to be sent to one of the other task units.

15. (Previously Presented) The hardware device of claim 12, wherein the source task unit is configured to activate the destination task unit.